

AMT630

Video Display Controller (Product Specification)

Version 1.0

2012.04

CONFIDENTIAL

ARKMICRO TECHNOLOGIES INC. reserves the right to change or modify the information contained herein without notice. It is the customer's responsibility to obtain the most recent revision of the document. **ARKMICRO** makes no warranty for the use of its products and bears no responsibility for any errors or omissions that may appear in this document.

Revision Record:

Date	Revision	Modification Description
2012-4-8	V1.0	Initial Version

CONFIDENTIAL

1. General Description

AMT630 is a highly integrated video control SoC with Digital LCD/TFT panel displaying controller and could support parallel RGB panel, sRGB panel, ITU656 panel, digital TCON and CPU panel. AMT630 integrates a video decoder and an Analog TFT-LCD Panel Control. It accepts analog NTSC / PAL / SECAM CVBS signals and S-Video from TV tuner, DVD, or VCR sources, including weak and distorted signals. Automatic gain control (AGC) and 9-bit 2-channel A/D converters provide high resolution video quantization, with automatic video source and mode detection. User can easily switch and adjust variety of signal source. Multiple internal adaptive PLL could precisely extract clock from video source and perform sharp-and-keen color demodulation. Build-in line buffer supports adaptive 2-D comb-filter, 2-D sharpening, and synchronization stable in a condense manner. Build-in On Screen Display (OSD) module is very flexible and easy programming. DC/DC, DC/AC, VCOM, etc. modules are cost effective for low cost and small area PCB solutions.

2. Features

Video Decoder

- ◆ Composite and S-Video Inputs; Multiple standards supported: NTSC and NTSC-Japan; PAL (B, D, G, H, I, M, N, etc.); SECAM;
- ◆ Four Analog Inputs: 1xCVBS+1xS-Video or 3xCVBS Inputs
- ◆ Analog and Digital AGC
- ◆ 9-Bit 2-Channel A/D Converters with Fixed Sampling Clock
- ◆ Only One Crystal (24 MHz) required for All Standards
- ◆ Internal PLL to Generate Video Clock
- ◆ Adaptive 2-D Comb Filter for Luminance and Chrominance Separation
- ◆ Precise Chrominance Demodulation
- ◆ Internal Buffers for Video Stability Control
- ◆ Video Noise Reduction

Video Enhancement

- ◆ Frequency Directive Sharpening
- ◆ Brightness, Contrast, Color, and Tint Adjustments
- ◆ Black-Level Extension and White-Level Extension
- ◆ Digital Chrominance Transient Improvement(DCTI) and Digital Luminance Transient Improvement(DLTI)
- ◆ 3-channel Gamma curve adjustment
- ◆ Green level enhancement
- ◆ Auto contrast adjustment
- ◆ Auto chrominance adjustment

Scaling Engine

- ◆ Support Digital panel with the resolution of 480x240, 640x240, 520x288, 800x480, 800x600, 1024x768, and more
- ◆ Support horizontal panorama scaling

- ◆ Support vertical panorama scaling

OSD Block

- ◆ Built-in 512-Character Font ROM (Including Special Font Characters)
- ◆ Dynamic OSD font RAM-----3072x12 (192 character) bytes
- ◆ 16 colors palette, support 5 OSD windows
- ◆ Support 16 color bitmap
- ◆ Blending with OSD Content and Video
- ◆ Blinking and Highlight Function
- ◆ Mirror image around Function

Interface

- ◆ Build-in parallel RGB panel, sRGB panel, digital TCON panel and CPU panel interfaces
- ◆ Digital RGB Independent Output Line-Inversion, Offset Control
- ◆ 8-Bit/10-Bit CCIR 656 Digital Video Output Format Support
- ◆ I2C-BUS interface (slave)

MCU

- ◆ Instruction fully compatible with industry standard 803x/805x, Fully static synchronous design
- ◆ High performance with 4 clock cycles per instruction cycle, up to 24MHz clock speed
- ◆ Program store in an external SPI Flash or E2PROM with ISP (In System Program)
- ◆ Build-in boot ROM support serial port configuration
- ◆ 2 Sets of Built-In PWM circuit: 2x16 bit and 3x11 bit
- ◆ Build-in 3 channels 10Bit ADC for serial key or other analog input
- ◆ Supports 13 standard interrupt sources include external interrupt, 3 Timer, Watchdog etc
- ◆ Programmable I/O ports (GPIO)
- ◆ I2C-BUS interface (master and slave)
- ◆ Hardware Remoter decoder support NEC and RC-5 IR code

Peripheral

- ◆ Build-in MCU & SPI Flash interface& E2PROM interface
- ◆ Support SPI FLASH and E2PROM on line program
- ◆ Build-in 10 Bit SAR ADC
- ◆ Build-in Display PLL
- ◆ Build-in LDO for 1.8v core power
- ◆ Build-in DC/DC controller which generate VGH (+15V) and VGL (-10V) of panel bias voltage
- ◆ Build-in DC/AC controller with over-voltage and open-Lamp protection make a low-cost back-light solution
- ◆ Programmable VCOM amplitude & Offset
- ◆ 3.3V Power Supply

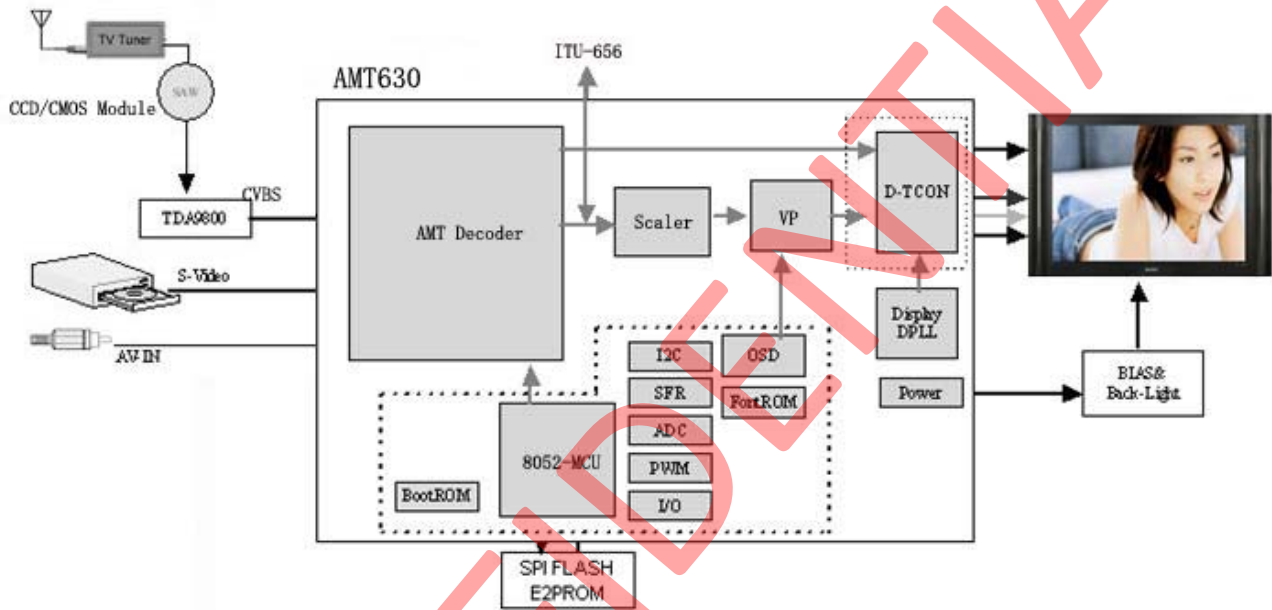
Package

- ◆ LQFP 64 Pin Package

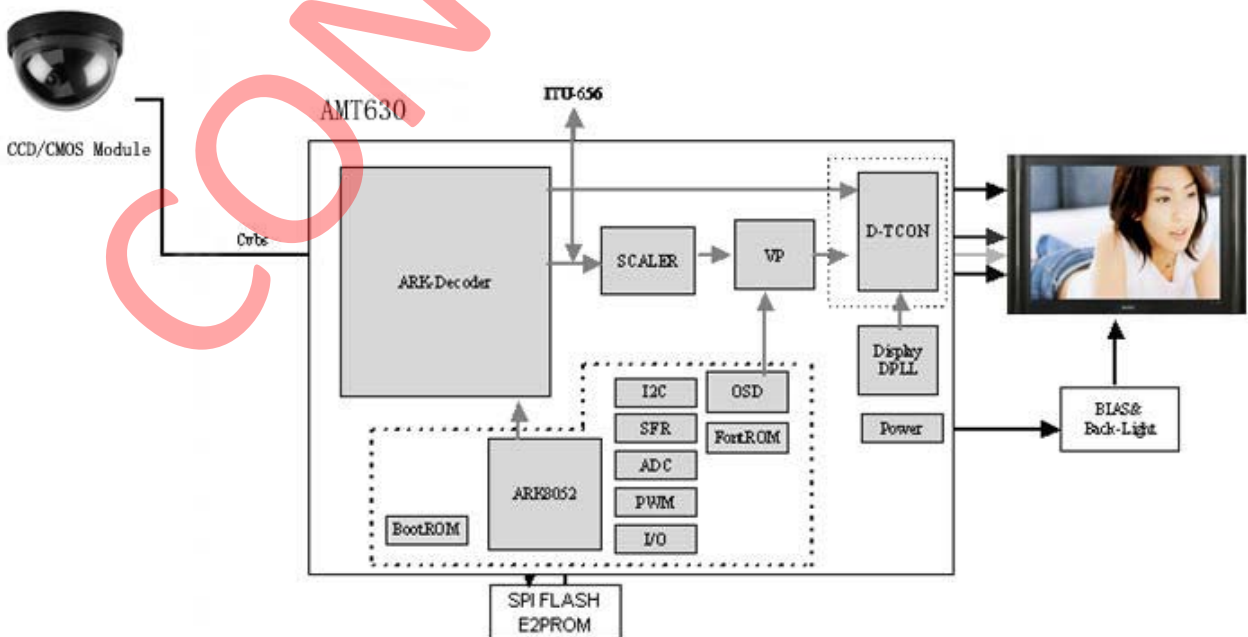
3. Application Field

- ◆ Car Reversing Monitor
- ◆ Visible Door Monitor
- ◆ Portable DVD / TV
- ◆ Small to medium sized LCD TV
- ◆ Other application using analog panel as the display unit

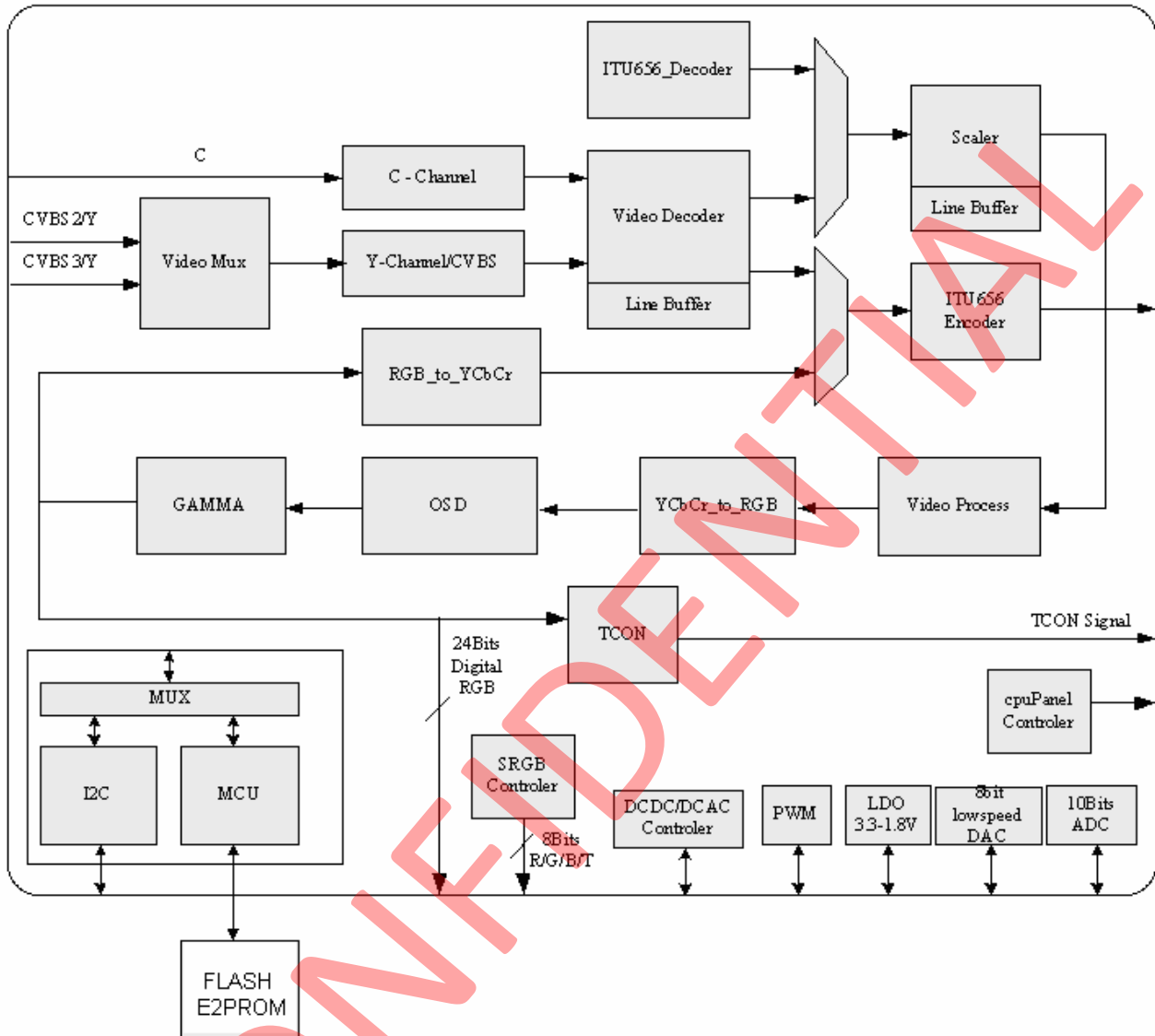
3.1 Portable-DVD, Portable-TV or Mini-TV



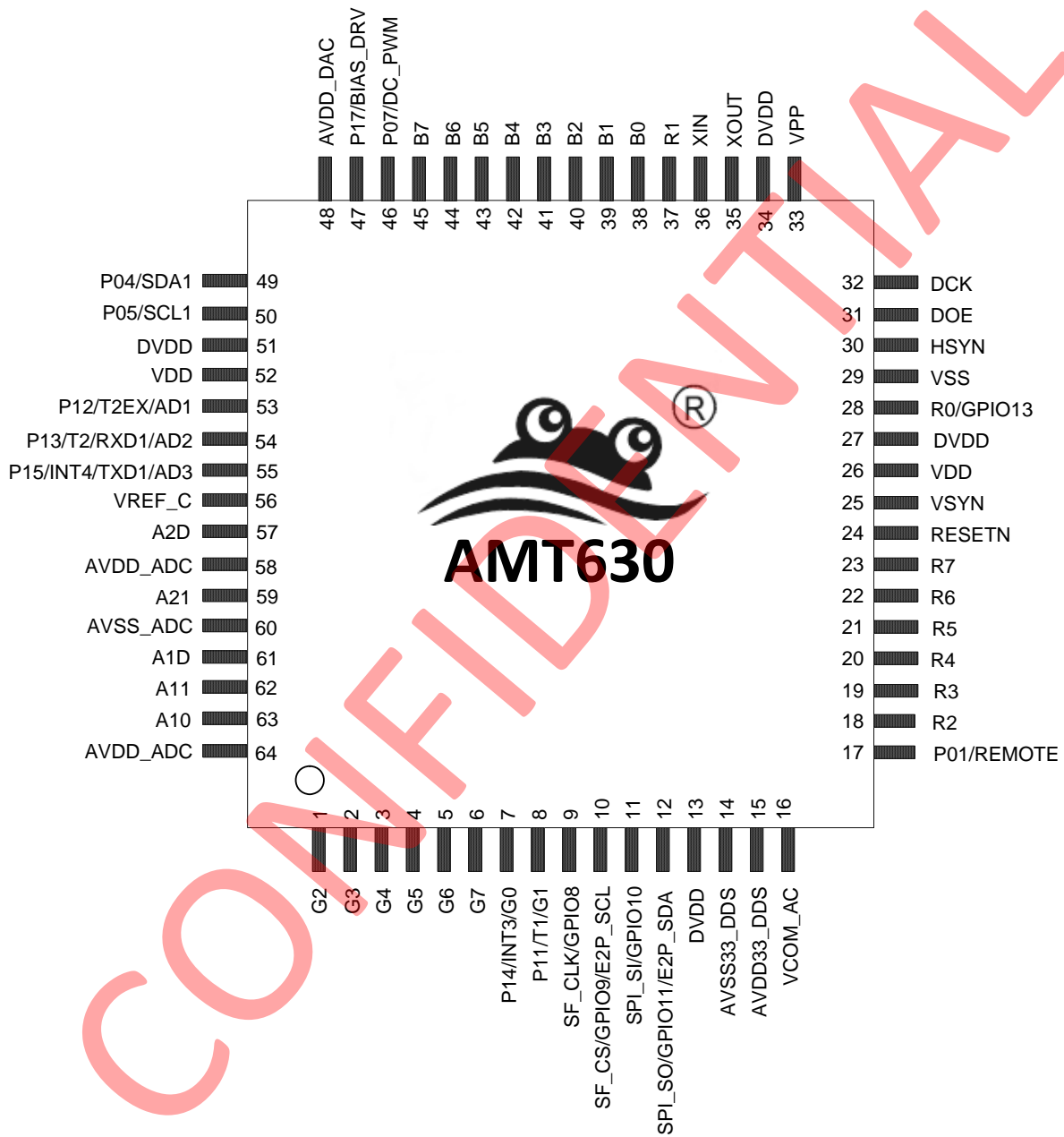
3.2 Visible Door Monitor/Car Reversing Monitor



4. Block Diagram



5. Pin Diagram



6. Pin Definition

PIN	TYPE	DESCRIPTION
1	IO	ITU_D0_P/GPIO0/G2/PWMA
2	IO	ITU_D1_P/GPIO1/G3/PWMB
3	IO	ITU_D2_P/GPIO2/G4/CPU_RST
4	IO	ITU_D3_P/GPIO3/G5/CPU_CS
5	IO	ITU_D4_P/GPIO4/G6/CPU_RD
6	IO	ITU_D5_P/GPIO5/G7/CPU_WR
7	IO	P14/INT3_N/DC_PWM/STVR/G0/ITU_D6/ITU601_HSYN
8	IO	P11/T1/CKV/PMODE/SRGB_DEN/G1/ITU_D7/ITU601_VSYN
9	IO	SF_CLK/PCLK/GPIO8
10	IO	SF_CS/PCEB/GPIO9/E2P_SCL
11	IO	SPI_SI/PEN/GPIO10
12	IO	SPI_SO/PDATA/GPIO11/E2P_SDA
13	P	DVDD
14	P	VSSD/VSS/AVSS33_DDS
15	P	AVDD33_DDS
16	IO	VCOM_AC/POL/SRGB_H
17	IO	P01/REMOTE
18	IO	R2/SD2/CPU_D0/TCPH3
19	IO	R3/SD3/CPU_D1/P20/STVR/SD0/ITU_D0/CKH3
20	IO	R4/SD4/CPU_D2/P21/PWMA/SD1/ITU_D1
21	IO	R5/SD5/CPU_D3/P22/PWMB/SD2/ITU_D2
22	IO	R6/SD6/CPU_D4/P23
23	IO	R7/SD7/CPU_D5/P24
24	I	RESETN
25	IO	(BOOT_UART)/STVL/VSYN/CPU_RD/SRGB_V/CPU_D6/SD4/ITU_D4
26	P	VDD
27	P	DVDD
28	IO	(BOOT_SPI)/TCPH1(LD)/GPIO13/SD0/R0/SD5/ITU_D5
29	P	VSS
30	IO	STHL/HSYN/CPU_CS/CPU_D7/SRGB_H/SD6/ITU_D6
31	IO	(BOOT_OTP)/TCPH4/DOE/CPU_RS/SRGB_DEN/SD1/SD7/ITU_D7
32	IO	CKH1/DCK/CPU_WR/CPU_D8/SRGB_CLK/ITU_CLK
33	P	VPP
34	P	DVDD
35	AOUT	XOUT
36	AIN	XIN
37	IO	G5/CPU_D9/GPIO19/STHR/R1
38	IO	G6/CPU_D10/GPIO20/SCL0/PWMA/B0/RXD2
39	IO	G7/CPU_D11/GPIO21/SDA0/PWMB/B1/TXD2

40	IO	B2/P32/CPU_D12
41	IO	B3/P33/CPU_D13
42	IO	B4/P34/CPU_D14
43	IO	B5/P35/CPU_D15
44	IO	B6/P36/CPU_D16
45	IO	B7/P37/CPU_D17
46	IO	DC_PWM/P07
47	IO	BIAS_DRV/P17/SRGB_V
48	P	AVDD_DAC
49	IO	P04/SDA1
50	IO	P05/SCL1
51	P	DVDD
52	P	VDD
53	IO	P12/T2EX/AD1
54	IO	P13/T2/RXD1/AD2
55	IO	P15/INT4/TXD1/AD3
56	AOUT	VREF_C
57	AOUT	A2D
58	P	AVDD_ADC
59	AIN	A21 (YC C in channel)
60	P	AVSS_ADC
61	AOUT	A1D
62	AIN	A11 CVBS IN
63	AIN	A10 CVBS IN
64	P	AVDD_ADC

7. Electrical Characteristics

7.1 DC Characteristics

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
DVDD	Digital IO supply voltage		3.0	3.3	3.6	V
I _{DVDD}	Digital supply current		--	50	60	mA
VPP	OTP Program supply voltage				6.5	V
AVDD_ADC	Analog ADC supply voltage		3.0	3.3	3.6	V
AVDD33_DDS	Analog DDS supply voltage		3.0	3.3	3.6	V
AVDD33_DAC	Analog DAC supply voltage		3.0	3.3	3.6	V
I _{AVDD}	Total analog supply current	CVBS input	40	50	60	mA

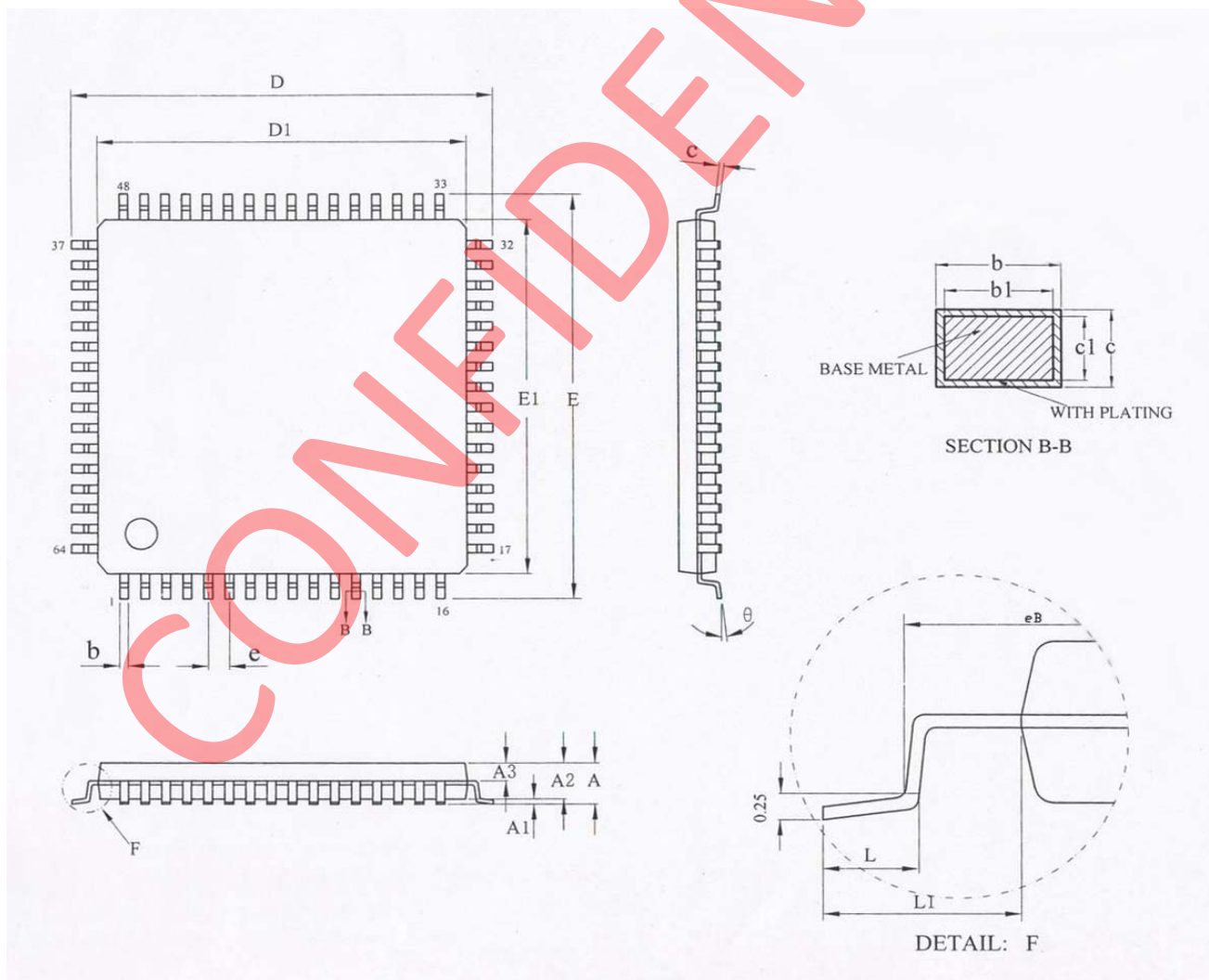
7.2 AC Characteristics

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Analog part						
Iclamp	Clamping current	VI=0.9VDC	--	+16	--	uA
Vi(p_p)	Input voltage (Peak-to-peak value)	For normal video levels 1V(p-p), 3dB termination 18/56 and AC coupling required; Coupling capacitor=22nF	--	0.7	--	V
Zin	Input impedance	Clamping current off	200	--	--	KΩ
Ci	Input capacitance		--	--	10	pF
@cs	Channel crosstalk	fi<5MHz	--	--	-50	dB
9-bit analog-to-digital converters						
B	Analog bandwidth	At -3dB	--	7	--	MHz
Φdiff	Differential phase		--	2	--	Deg
Gdiff	Differential gain		--	2	--	%
Fadc	ADC clock frequency		13.5	27	54	MHz
DNL	DC differential linearity Error		--	0.7	--	LSB
INL	DC integral linearity error		--	1	--	LSB
PLL						
FOUT	PLL output range		--	--	480	MHz
FIN	Input reference frequency range		1	--	24	MHz
Fvco	VCO frequency range		--	--	480	MHz
Tjitter	Timing Jitter Peak to Peak		--	88	--	Ps
Tjitter rms	Timing Jitter RMS		--	18	--	Ps
10BIT SAR ADC						
resolution			--	10	--	BIT
Vi(p_p)	input voltage (peak-to-peak value)		--	2	3.3	V
Fadc	Sample clock		--	--	1	MHz
INL	DC integral linearity error		--	--	+2	LSB
DNL	DC differential linearity error		--	--	+2	LSB
Digital inputs						
VIL(n)	Low-level input voltage		0		0.4	V
VIH(n)	High-level input voltage		2.4		3.6	V

Digital outputs						
VOL	Low-level output voltage		0		0.4	V
VOH	High-level output voltage		2.4		VCC+0.5	V
Temperature						
TA	Ambient Operation Temperature		0		70	°C
TSTG	Storage Temperature		-40		125	°C
Tj	Junction Temperature				125	°C

8. Package

AMT630 is packaged in a 64 Pin LQFP package.



SYMBOL	MILLIMETER		
	MIN(mm)	NOR(mm)	MAX(mm)
A	-	-	1.60
A1	0.05	-	0.20
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.17	-	0.25
b1	0.16	0.18	0.20
c	0.13	-	0.18
c2	0.12	0.127	0.14
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
eB	8.10	-	8.25
e	0.40BSC		
L	0.40	-	0.65
L1	1.00BSC		
θ	0	-	7°
L/F (mil)	160x160		
	210x210		

CONFIDENTIAL